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# Component wise contribution to total thermal resistance in 2D material based device stacks



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#### ABSTRACT

Vertically stacked devices is a promising direction in future electronics. However, a major thermal bottleneck to such vertical integration is dissipated heat generation within the stack. It is shown that the interface between two-dimensional (2D) materials and substrates is a limiting factor, for heat flow, in constituting electrical devices. Through considering the example of a graphene-based platform, the thermal boundary conductance (TBC) along with the converse thermal resistance ( $R_K$ ) was estimated through a diffuse mismatch model considering the related phonon dispersion. It was shown, for instance, that the graphene-SiO<sub>2</sub> interface contributes to more than 50% of the  $R_K$  in a graphene-SiO<sub>2</sub>-Si assembly. Weak van der Waals interactions at the interface coupled with phonon frequency mismatch are attributed as the reasons for the reduced TBC, allowing less heat to flow across the interface. This study provides a guideline on effect of materials and layouts on thermal efficiencies of 2D material based device stack.

### 1. Introduction

With the proposed use of a single-to a few-atom thick 2D materials in electronic, optoelectronic and thermoelectric device applications [1-3], interfaces between these materials and their substrates may be a potential bottleneck for heat flow. This is from the point of view that the dimensionality and related volume of a 2D material is similar to the interface. Broadly, when a 2D material is grown on or transferred onto a 3D substrate, van der Waals (vdW) forces at the interface are typically two-three orders of magnitude lower in comparison to strong, e.g., covalent, bonding [4]. Such weak coupling leads to a temperature drop across the interface ( $\Delta T$ ), which for a given thermal energy transfer (= Q), yields a thermal resistance  $(R_K = \Delta T/Q)$  to heat flow across the interface. The inverse of the  $R_K$  is the thermal boundary conductance  $(\text{TBC}) = 1/R_K$ , which per unit area, has the units of W/m<sup>2</sup>K. Broadly, the *net R* is constituted from both (a) the related thermal conductivity ( $\kappa_{2D}$ ), as well as the (b) degree of thermal coupling [5-7] between the 2D materials and the substrate. We focus on the in-plane value of the  $\kappa_{2D}$  $(=\kappa_{\parallel})$  as generally the cross-plane value  $(=\kappa_{\perp})$  is much smaller, *e.g.*, in graphite considered to be constituted from many loosely coupled single 2D layers, the  $\kappa_{\parallel}$  of 2200 W/m.K is significantly larger compared to the  $\kappa_{\perp}$  of 6 W/m.K, presumably due to weak interlayer coupling [8-10]. The

 $\kappa_{\parallel}$  is expected to be a strong function of the constituent phonon dispersion [11], and may also be influenced by the 2D material configuration (monolayer *vs.* multilayer) and termination, *e.g.*, whether the edges are zigzag, armchair, *etc.* The experimental determination of the  $\kappa_{2D}$  is also generally dependent on the methodology of measurement, *i.e.*, suspended [12-16], supported [17], contact [18] *vs.* non-contact [12,19], *etc.* 

Generally, the  $\kappa_{2D}$  of 2D materials both in isolation (*i.e.*, in a suspended form), *e.g.*, graphene, transition metal dichalcogenides (TMDCs), MXenes, *etc.* as well as through measurements of films on substrates have been widely reported and have been summarized, through a literature survey, in Fig. 1. The related lattice thermal conductivity is formally expressed through:

$$x_{2D} = \sum_{j} C_{j,q} v_{g_{j,q}}^{2} \tau_{j,q} \dots$$
 (1)

Here, the *j*th contributing mode, *e.g.*, the phonon, in the *q*th direction is considered for the specific heat capacity  $(C_{j,q})$ , the phonon group velocity  $(v_{gj,q})$  and the relaxation time  $(\tau_{j,q})$ . There is also a correlation of the thermal conductivity with the Grüneisen parameter  $(\gamma)$  - typically [20] in the range 1–3, which is a measure of the extent of lattice anharmonicity, *e.g.*, a large  $\gamma$  may yield an ultralow  $\kappa_{2D}$ . From Fig. 1 (a),

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**Fig. 1.** Thermal conductivity of representative 2D materials. (a) In plane thermal conductivity ( $\kappa_{\parallel}$ ) of 2D layered materials from experimental measurements at room temperature. The 2D materials and their configuration, *i.e.*, suspended, supported, *etc.* are indicated. The data are representative of CNT/ graphene (suspended) [13,14,27,28,29], CNT/graphene (supported) [12,30], h-BN [31], WS<sub>2</sub> [38], MoS<sub>2</sub> [32-36], ReS<sub>2</sub>[25], black P [37], WSe<sub>2</sub> [39], MoSe<sub>2</sub> [40], Silicene [41], Stanene [42], WTe<sub>2</sub> [43], HfTe<sub>2</sub> [44], ZrTe<sub>5</sub> [44], BCN [45], Te [26], SnSe [21,22], In<sub>2</sub>Se<sub>3</sub> [46], and SN<sub>2</sub>Bi [47], etc. (\*) indicate theoretical estimates. (b) Thermal conductivity of 2D materials, for which the in-plane thermal conductivity ( $\kappa_{\parallel}$ ) and cross-/through-plane thermal conductivity ( $\kappa_{\perp}$ ) have been experimentally determined. The data are representative of graphite [48], WS<sub>2</sub> [38], ReS<sub>2</sub> [25], MoS<sub>2</sub>[49, 50], WSe<sub>2</sub> [38], MoSe<sub>2</sub> [40], HfTe [44], ZrTe<sub>5</sub> [44], Te [26], SnSe [21], and WTe<sub>2</sub>[43]. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

materials with low thermal conductivity such as SnSe, have low average  $v_g$  (1420 m/s) and large  $\gamma$  of more [21,22] than 3. Alternately, for graphene, the higher  $v_g$  (of ~3200 m/s) and smaller  $\gamma$  (~2) leads to higher  $\kappa_{2D}$ . Considering engineering rules of thumb, materials constituted from lighter atoms yield higher  $v_g$  and together with bonding stiffness, as in a covalent bond, may lead to higher  $\kappa_{2D}$ [15], *e.g.*, compound 2D materials with P or S, have higher  $\kappa_{\parallel}$  compared to those with heavier elements, such as Se or Te. For instance, the  $\kappa_{\parallel}$  of WS<sub>2</sub>, WSe<sub>2</sub> and WTe<sub>2</sub> decrease successively in the order 124 W/m.K, 40 W/m.K and 9 W/m.K, respectively [23,24]. The thermal conductivity of 2D materials also depend on anisotropy, as indicated in Fig. 1 (b). The typically lower value of the  $\kappa_{\perp}$  can be attributed to weak interlayer bonding, which leads to reduced cross-plane  $v_g$ . Crystallographic symmetry can also yield

varying  $\kappa_{\parallel}$ , *e.g.*, ReS<sub>2</sub>, and Te show higher  $\kappa_{\parallel}$  in the longitudinal direction [25,26]: Fig. 1(b), possibly due to charge density wave formation. The  $\kappa_{\perp}$  seems to be relatively unaffected by *in-plane* symmetry considerations as the  $\nu_g$  along the through plane direction is independent of the in-plane orientations. Consequently, in this work, we consider only  $\kappa_{\perp}$  as relevant for the *cross-plane* heat transfer.

When the 2D layers are placed on bulk, *i.e.*, three-dimensional (3D) substrates, the measured TBC has been typically reported to be in a wide range, presumably due to dimensional mismatch at the interfaces: Fig. 2. For example, for a single layer graphene (SLG) and multilayer graphene (MLG) placed on SiO<sub>2</sub>/Si substrates, the TBC is in the range [7,51,52] of  $25-50 \text{ MW/m}^2$ . K, and is typically higher in the MLG samples where additional layers enhance interfacial transmission through additional flexural phonon branches [53-55]. Indeed, it was interesting to note that the TBC related to the 2D material/3D bulk interfaces: Fig. 2(a), seems to be smaller compared to the TBC of 3D/3D interfaces: Fig. 2(b). For example, the TBC of graphene/SiO2 near room temperature (~25  $MW/m^2$ . K) is half that of Si/SiO<sub>2</sub> interface (~48 MW/m<sup>2</sup>. K). The measured TBC in the former case is equivalent to the thermal resistance of ~56 nm thick amorphous SiO<sub>2</sub>, assuming a  $\kappa_{SiO2}$  of 1.4 W/m.K. In comparison, the equivalent  $R_K$  of most 3D/3D solids yields an equivalent SiO<sub>2</sub> thickness in the range of  $\sim$ 10–30 nm.

The experimentally reported highest TBC is 14 GW/m<sup>2</sup>. K for Pd-Ir [51] and lowest TBC is 6 M W m<sup>-2</sup> K<sup>-1</sup> for graphene/diamond [8, 51]. Generally, a metal-metal interface has a higher TBC, as electronic conduction is more significant than lattice thermal conductivity. While diamond exhibits one of the highest thermal conductivity of 3D solids (~2200 W/m.K), it bonds very weakly with other materials at interface, which leads to the low TBC. The lower end of TBC occurs typically with those materials of highly dissimilar lattice spectra, with anharmonic processes dominating the heat flow at interface.

The TBC also seems to depend on process parameters such as material deposition rate and base pressure [23], *e.g.* for Ti (an excellent oxygen getter) on graphene, the TBC has a larger range at  $32-65 \text{ MW/m}^2$ . K. Generally, a slow materials deposition rate also seems to improve TBC through increasing the interfacial quality and through less material defects. Other important TBC determining parameters are related to (a) phonon frequency mismatch at interface, (b) interface quality and cleanliness, and (c) interface bonding, all of which have been shown to modulate the TBC by 50% or more [35,51,56,57].

In this work, we further investigate the parameterization of the  $R_K$  of a 2D film/substrate stack, of possible utility in nanoscale devices, through the domination of the  $R_K$  by the relevant interface. We focus on the graphene-SiO<sub>2</sub>-Si stack, while discussing the choice of alternate 2D materials and substrates, with respect to the  $R_K$ . The new findings in our study are analyses of component wise contribution of thermal resistances in 2D material-based device stack. This includes graphene/ oxide DMM calculation and analysis of each component. It was found that there is less work done on overall thermal resistance of device stack and our research aims to contribute to related avenues of investigation. Also, while experimental measurements can provide a lumped-value of the TBC, it cannot be readily separated into their comprising parts. Consequently, through DMM calculation of graphene/SiO2 based materials and related interfaces we have attempted to provide adequate attention to other components of the net thermal resistances incorporating thin film/substrate interfacial resistance (e.g. Si/SiO<sub>2</sub>), as well as the 2D and substrate material's intrinsic resistances (e.g. graphene, Si and  $SiO_2$ ). We also consider the factors that affect these components, such as thickness, as well as the material and interface quality. Our analysis provides a guideline for efficient thermal design and heat management of 2D material-based devices. The bottom Si in the graphene-SiO<sub>2</sub>-Si stack may be considered with respect to either (a) a bulk Si substrate (~500 µm thick), or (ii) a Si device layer (~100 nm thick) in a Silicon-on-Insulator (SOI) architecture. Given the much larger thickness of the Si substrate, in the first case, it is obvious that the net R = t/t $\kappa_{bulk} \sim 3 \times 10^{-6} \text{ m}^2 \text{ K/W}$ ) for the overall device would be dominated by



**Fig. 2.** Comparison of thermal boundary conductance (TBC) at **(a)** 2D/3D bulk substrate interfaces, and **(b)** 3D/3D interfaces. Black solid lines are calculated TBC, estimated through the diffuse mismatch model (DMM). Colored points are experimental data [5,18,23,32,35,56-59] near 300 K. Dashed lines related to an equivalent thickness of SiO<sub>2</sub> are indicated.

the substrate. In the second case, i.e., with oxide thicknesses of the order of 1000 nm in SOI wafers, the R particular to the SiO<sub>2</sub> would again be of a similar order of magnitude. Consequently, our explanations and analyses pertain to a specific case, where such larger R may not be relevant, e.g., through lift-off from the substrate and subsequent transfer onto a medium which does not pose thermal resistance related bottlenecks. In our analysis, we then use a token Si thickness of 100 nm, and a native oxide of  $\sim 1$  nm, to indicate the relative order of magnitude  $R_{\rm F}$  posed by the 2D material-oxide interface, *i.e.*, the prototype graphene-SiO<sub>2</sub>-Si device stack. We consider 100 nm thickness for 2D materials-based device because the heat removal in such device is mainly cross-plane through the substrate which can be taken as critical length scale over which the heat travels in the lateral direction before sinking to the substrate is around 100 nm [35,60]. We calculated this critical length, known as lateral thermal healing length,  $L_H = \sqrt{k_{2D} t_{2D} / TBC}$ . For our graphene stack  $L_H$  is on the order of 100 nm.

# 2. Results and discussion

The component-wise contribution to the total *R* of a single layer graphene (SLG)-SiO<sub>2</sub>-Si stack in Fig. 3. The *net R* of the SLG/SiO<sub>2</sub>/Si stack was modelled through a series resistance approach:

$$R_{total} = R^{SLG} + R_K^{SLG/SiO_2} + R_K^{SiO_2} + R_K^{Si/SiO_2} + R_K^{Si}$$
(2)

Here,  $R^{SLG}$  is the intrinsic resistance of SLG,  $R_{K}^{SLG/SiO_{2}}$  is the resistance

of the SLG/SiO<sub>2</sub> interface,  $R^{SiO_2}$  is the intrinsic resistance of SiO<sub>2</sub>,  $R_K^{Si/SiO_2}$  is the resistance of Si/SiO<sub>2</sub> interface, and  $R^{Si}$  is the intrinsic resistance of Si.

We first consider the material intrinsic resistances. The  $R^{SLG}(=t/\kappa_{\perp})$ , where *t* is the effective SLG thickness of ~0.34 nm and with  $\kappa_{\perp} = 6$  W/m. K, contribution to the *net R* is smaller by around two orders of magnitude compared to the other components. For example, the intrinsic *R* for the SLG is  $\sim 5 \times 10^{-11}$  m<sup>2</sup> K/W – also see sensitivity contour plots considering variations in the  $\kappa_{\perp}$  and *t* in Figure S1. The  $R^{SiO_2}$  and  $R^{Si}$  were estimated from the ratio  $t/\kappa$ , to be of the order of  $2 \times 10^{-8}$  m<sup>2</sup> K/W and 3  $\times 10^{-9}$  m<sup>2</sup> K/W, respectively – also see Figure S2 related to the possible variability [61] of  $\kappa_{SiO2}$ . We follow typical device structure, as may be deployed for Si in a SOI platform, and assume  $t_{SiO_2} = 1$  nm and  $\kappa_{\perp SiO2} =$ 1 *W*/*m.K*, and for Si we assume  $t_{Si} = 100$  nm with  $\kappa_{\perp, Si} = 30$  W/m.K [62,63]. We note that  $\kappa_{\perp, Si}$  reduced from bulk value (~148 W/m.K) at such a scale –see Figure S3 for thickness dependence of  $\kappa_{Si}$ . Our linear length dependence of  $\kappa_{Si}$  works well in sub-micron range. Above 1 µm thickness, phonon mean free path (MFP) is enhanced and  $\kappa_{Si}$  starts to increase exponentially, per the Fuchs-Sondheimer relation, and eventually reaches the bulk value (of ~140 W/m.K) [71]. Indeed, the related MFP varies significantly across the phonon spectrum. Recent studies indicate that MFP of Si ranges [55,64-66] from 0.3 to 8.0 µm and would be less than 10 nm for SiO<sub>2</sub>. While lower values of  $\sim$ 300 nm have been reported for Si, the net material thermal conductivity should also incorporate contributions of phonons with a broader distribution of



Fig. 3. The net thermal resistance (*R*) of a graphene/SiO<sub>2</sub>/Si stack. (a) Schematic view of the stack with (b) constituent thermal resistance components, the magnitudes of which are indicated by the relative size of the boxes in the stacked column.

MFPs. For instance, phonons with MFP  $>1 \mu m$  (low-energy acoustic phonons minimally affected by Umklapp scattering [67]) may contribute significantly to heat conduction in Si.

The two primary analytical models for expressing phonon transport across the interface are the Acoustic Mismatch Model (AMM) and the Diffuse Mismatch Model (DMM) [51,68,69]. AMM treats incident phonon reflection incorporating plane wave based transport, and the materials in which the phonons propagate are treated as elastic continua. The transmission probabilities of phonons are estimated from the acoustic impedances on each side of the interface. A key assumption related to the AMM is that no scattering occurs at the interface. The assumptions of wave nature of phonon transport and specular scattering at the interface make the assumptions related to the AMM more pertinent when predicting TBC at low temperatures and at ideal interfaces [69]. However, at room temperature, the TBC in most materials is dominated by phonons with wavelength comparable to interatomic distances. Thus, the AMM is generally not appropriate for room temperature solids, though it may correctly describe the behavior of some low frequency phonons that are significant at low temperatures. In contrast, for, the DMM, completely diffuse scattering at the interface may be assumed: a scattered phonon has no memory of its modes (longitudinal or transverse). The transmission probabilities of phonons are determined by the mismatch of the phonon density of states (PDOS) on each side of the interface. The key difference between these models is then that the AMM is more appropriate at low temperatures where the related phonons have wavelengths longer than the roughness of the interface [51]. The interface may then be treated as a plane where the phonons scatter specularly. Alternately, the DMM does account for interface roughness and phonons are diffusely scattered at interface, with no memory of their incoming polarization and subsequent trajectory after scattering at the interface. Since most thermal transport for device applications is above room temperature, here we choose DMM.

We performed DMM calculation using MATLAB(R). The details of the DMM simulation are presented in Supporting information. We estimated the  $R_{th, SLG/SiO_2}$  and the  $R_{th, SI/SiO_2}$  as  $\sim 5 \times 10^{-8} \text{m}^2$  K/W and  $\sim 2.6 \times 10^{-8} \text{m}^2$ K/W DMM [51]. Through the TBC, which between two materials can be generally expressed as

$$TBC\left(=\frac{1}{R_{th}}\right) = \sum_{j} \int_{0}^{\omega_{max,j}} \hbar\omega \, v_{j,1} \frac{df(\omega, T)}{dT} D(\omega) \, \alpha \, d\omega \tag{3}$$

where h is the reduced Planck's constant,  $\omega$  is angular frequency, v is the phonon velocity,  $f(\omega, T)$  is the Bose-Einstein distribution function, *T* is the temperature, d ( $\omega$ ) is the phonon density of states (DOS). The *j* refers to an acoustic phonon (longitudinal and transverse) branch. The integration is performed with respect to a maximum cutoff frequency ( $\omega_{max}$ , *j*) for the *j*<sup>th</sup> branch, considered up to the limit of the first Brillouin zone (FBZ). The  $\alpha$  is a mode transmission coefficient =  $H_2/(H_1+H_2)$ , where  $H = \frac{1}{2} \sum_{j=1}^{\omega_{maxj}} \int_{-\infty}^{\infty_{maxj}} h_{ij} w_{ij} f(\omega, T) D(\omega) d\omega$  is the incident phonon flux from the

$$H = \frac{1}{4} \sum_{j} \int_{0} \hbar \omega \, v_{j,1} f(\omega, T) D(\omega) d\omega, \text{ is the incident phonon flux from the}$$

corresponding material (1 or 2) and is in the range of 0–1. We neglect optical branches as they were not considered to contribute much [11] (*e.* g., at~12% of the total TBC for Si [62]) to the phonon transport due to their negative group velocity as evident from related phonon dispersion diagrams as well as shorter lifetimes relative to acoustic phonons [51].

We first consider a Debye-like model, where the energy distribution may be considered isotropic, as is typically assumed for Si and SiO<sub>2</sub> for an estimate of the DOS [46]. A truncated Debye model was assumed along with a linear dispersion for phonons [57]. The cutoff frequencies ( $\omega_{max, j}$ ) of the longitudinal acoustic (LA) and transverse acoustic (TA) phonon modes was considered at the BZ boundary in the [100] direction. It was assumed that scattering at the interfaces is elastic and allow for mode conversion [50] at the interfaces. For graphene/SiO<sub>2</sub> we follow the suggestions related to the modification of the DOS from Duda *et al.* 

[68], anisotropic phonon dispersion modification from Chen *et al.* [71] and phonon group velocity modification from Li et al. [70] for anisotropic layered materials and will be further discussed in the following sections. We choose to follow ref. 44-46 assumption to improve accuracy of the TBC of graphene/SiO<sub>2</sub> within the same order of magnitude. The original derivation of the DMM proposed by Swartz et al., is generally applicable for isotropic solids [50]. However, for anisotropic materials like graphene, traditional isotropic DMM overestimates TBC by three order of magnitude. In order to account for the anisotropy, we follow the suggestions related to the modification from Duda et al. [68] where the authors modified TBC for metal/graphite interface by using effective 2D Debye DOS. This 2D DOS model still overpredicts TBC of graphene/metal by an order of magnitudes. Consequently, we deployed an anisotropic Debye dispersion yielding a significant improvement on the isotropic model, with results much closer to experimental values. However, anisotropic Debye dispersion gives inaccurate approximations of the group velocity and cutoff frequencies of 2D materials [71]. Therefore, we have used a truncated linear dispersion [70] for velocity modification to accurately predict TBC of graphene/SiO<sub>2</sub> for comparison to experimental results.

We estimated the phonon density of states of the graphene [68], as  $\omega/(2\pi v_{g,j}^2 d)$ , where d (~0.34nm). The in-plane  $v_g$  was used for the DOS calculation, while the cross-plane  $v_g$  for each phonon polarization in the direction of transport were used for estimating the  $\alpha$ . The respective values of the  $v_g$  are listed in Table S1. An anisotropic phonon dispersion relevant to 2D materials [70], of the form:  $\omega^2 = v_a^2 k_a^2 + v_b^2 k_b^2 + v_c^2 k_c^2$ , was used where a and b refer to the basal plane axes direction and c refers to the out-of-plane axis. It was assumed, for graphene, that  $v_a=v_b$ . Such a modification yields an ellipsoidal BZ. In the evaluation of phonon flux for TBC of LA, TA, and ZA phonons, we follow Chen *et al.* [71] to consider the quasi-LA and quasi-TA modes, as TL1 and TL2 quasi-modes. The TL1 (/TL2) branch is constituted from TA (/LA) phonons along the c axis and LA (/ZA) phonons in the a-b plane, respectively. The corresponding  $v_g$  and  $\omega_{max, j}$  are given in Table S1.

The phonon velocity for the LA and TA phonons were estimated from a linear dispersion of the corresponding branches [72], where phonons of frequency up to  $\omega_{max,i}$  were assumed to have a fixed velocity derived from the elastic constants [70] of the graphite. *i.e.*, with  $C_{11}$ =1060GPa,  $C_{44}$ =4.2GPa,  $C_{66}$ =450 GPa. The  $\omega_{max,j}$  were considered at the boundaries of the BZ, with the cut-off frequency along the *a-b* plane obtained from the average at the high-symmetry M and K points [70], and that along the perpendicular c axis obtained from the high symmetric A' point (see Figure S4 in Supporting Information) after unfolding the phonon dispersion along the *c* axis [46]. The unfolding was done in real space by cutting the four-atom-basis primitive unit cell in half along the *c* axis to form a unit cell with a two-atom basis [71]. The dispersion relation [59] in the *c*-axis direction is continuous at the FBZ boundaries, *e.g.*,  $TA \rightarrow TO'$ and LA→LO' (from Figure S4 in Supporting Information) whereas along the *a*-*b* plane the dispersion relation shows gaps at the BZ boundary and has low velocity optical modes, compared to the acoustic counterparts. The  $v_g$  for ZA phonons was estimated using a piecewise approximation to the phonon dispersion [70], e.g., the ZA phonon branch was divided into two linear segments, with the phonon velocity calculated (i) from  $C_{11}$ , in the first segment, and (ii) from a fit to the experimental dispersion, in the second segment. The second cut-off frequency  $\omega_{ZA, ab2}$  (see Figure S4) was derived from the averages of the phonon frequencies and wavevectors at points M and K at the FBZ boundaries [70]. The first cut-off frequency  $\omega_{ZA, ab1}$  was determined from the intersection of two lines in the piecewise linear dispersion. The corresponding  $v_g$ ,  $k_{cutoff}$  and  $\omega_{max,j}$ are given in Table S1. Such a phonon velocity modification provides more accurate results compared to the "secant" method, i.e., from the slope of the line connecting the  $\Gamma$  to the end of the FBZ.

The related phonon flux of each branch of graphene can then be expressed as,

$$H_{TA/TL1} = \sum_{j} \frac{k_B^4}{8\pi^2 \hbar^3} \left\{ \frac{1}{v_{ab,1}^2} \int_{0}^{x_{max,cj}} \frac{T^4 x^3}{e^x - 1} dx + \int_{x_{max,cj}}^{x_{max,cj}} \left[ \frac{\theta_{D,abj}^2 \theta_{D,cj}^2}{\theta_{D,abj}^2 - \theta_{D,cj}^2} \frac{T^2 x}{e^x - 1} - \frac{\theta_{D,cj}^2}{\theta_{D,abj}^2 - \theta_{D,cj}^2} \frac{T^4 x^3}{e^x - 1} \right] dx \right\}$$
(4)

$$H_{TL2} = \sum_{j} \frac{k_{B}^{4}}{8\pi^{2}\hbar^{3}} \left\{ \frac{1}{v_{ab,1}^{2}} \int_{0}^{x_{max,ab,1}} \frac{T^{4}x^{3}}{e^{x} - 1} dx + \frac{1}{v_{ab,2}^{2}} \left[ \int_{x_{max,ab,j}}^{x_{max,ab,j}} \frac{T^{4}x(x - \Delta x)^{2}}{e^{x} - 1} dx + \int_{x_{max,ab,j}}^{x_{max,ab,2}} \frac{\hbar^{2}v_{ab,2}^{2}k_{ab,2}^{2}}{e^{x} - 1} - x(x - \Delta x)^{2} \frac{T^{4}x(x - \Delta x)^{2}}{e^{x} - 1} dx \right] \right] \right\} \dots$$
(5)

where  $k_B$  is Boltzmann constant,  $x = \hbar \omega / k_B T$ ,  $O_{D,cb,i}$ ,  $O_{D,c,j}$  are the Debye temperatures along the *a-b* plane and *c* direction respectively,  $v_{ab,1}$  and  $v_{ab,2}$ , are the phonon velocities along the *a-b* plane, and  $k_{ab,1} k_{ab,2}$  are the cut-off wavevectors at  $\omega_{ZA, ab1}$  and  $\omega_{ZA, ab2}$  respectively, determined from the relationship  $k_{ab}^2 k_c = 6\pi^2 \eta$ , where  $\eta$  is number density of primitive unit cells, corresponding to the first and second segment of ZA branch,  $\delta x = \hbar k_{ab,1}$  ( $v_{ab,1} - v_{ab,2}$ )/ $k_B$ T. The parameters deployed in this model are listed in Table S1.

Using such a modified anisotropic DMM, it was found that at room temperature, that the TBC was~ 20 MW/m<sup>2</sup>. K, for the SLG/SiO<sub>2</sub> interface, and~38 MW/m<sup>2</sup>. K, for the Si/SiO<sub>2</sub> interface, respectively. These values are to be compared with the experimentally determined values [19,57] of 25 MW/m<sup>2</sup>. K and 48 MW/m<sup>2</sup>.K, respectively: Fig. 2 (a). We note that the TBC of graphene/SiO<sub>2</sub> in an alternate experimental report [6], indicated by unfilled red points in Fig. 2 (a), were estimated using graphene encapsulated with SiO<sub>2</sub> both on the top and bottom and exhibits higher TBC compared to the bare graphene/SiO2 case. As indicated earlier, a lower TBC may be related to dissimilar phonon dispersion spectra. We compared our DMM results to related experimental measured TBC to gain new insight on TBC dependence on different 2D materials and substrates. First, we find from Fig. 2(a) DMM prediction has better agreement with the experimental measurements when a 2D material is placed on a bare substrate compared to enclosed by thin films. This also indicate that the DMM calculations for 2D materials gives close fit when the experimental measurement is taken using non-contact methods (like TDTR) in comparison to contact methods  $(3-\Omega)$ . For example, our DMM results match closely with bare graphene/SiO<sub>2</sub> [6], but vary significantly with encased graphene/SiO<sub>2</sub><sup>34</sup>. Moreover, we find that the TBC related to the 2D material/3D bulk interfaces is smaller compared to the TBC of 3D/3D interfaces (Fig. 2(a) and (b)). For example, the TBC of graphene/SiO<sub>2</sub> near room temperature  $(\sim 25 \text{ MW/m}^2 \text{ K})$  is half that of Si/SiO<sub>2</sub> interface ( $\sim 48 \text{ MW/m}^2 \text{ K}$ ). The measured TBC in the former case is equivalent to the thermal resistance of ~56nm thick amorphous SiO<sub>2</sub>, assuming a  $\kappa_{SiO2}$  of 1.4W/m.K. In comparison, the equivalent R of most 3D/3D solids yields an equivalent  $SiO_2$  thickness in the range of ~10–30nm. These factors have practical implication for efficient thermal design and heat management of 2D material-based devices.

It is also to be noted that experimental TBC can be modulated by both *extrinsic* and *intrinsic* factors. In table S2 we provide examples of the *extrinsic* factors different effective processing techniques. to the deployed experimental techniques, such as (a) applied pressure between the disparate materials - which increases the TBC, *e.g.*, a linear increase was seen for 2D/3D interface [7,58] under a pressure of 8GPa, as related to Al/graphene/SiO<sub>2</sub>/SiC from 30 MW/m<sup>2</sup>. K to 200 MW/m<sup>2</sup>. K, (b) layer encapsulation, *e.g.*, the TBC of (bare) graphene on bulk SiO<sub>2</sub> substrate was increased three-fold by encapsulating the graphene with 30nm SiO<sub>2</sub><sup>24</sup>; here, the additional layer increases the coupling of the low frequency flexural mode of the 2D material with the encapsulating layer's surface phonon mode increasing the TBC. (c) chemical functionalization, yielding covalent bonding at the interface, *e.g.*, through

treating graphene with oxygen [56], (d) interface roughness and cleanliness, *e.g.*, the TBC of SiC/SiO<sub>2</sub> at  $\sim$ 12 MW/m<sup>2</sup>. K is a factor of four lower than that in Si/SiO [57], due to a larger surface roughness of the SiC ( $\sim$ 3–5nm), along with large number of vacancy defects, causing increased phonon scattering, as well as (e) *fabrication techniques*, *e.g.*, graphene on a Cu substrate has a lower TBC of  $\sim$ 35% compared to transferred graphene [18], perhaps due to a better conformality in the former case. It was also seen that annealing of the transferred graphene can yield improvement in the TBC, perhaps due to an enhanced contact area between 2D material and substrate [73].

We note that these experimental results for a particular 2D-3D substrate set may not improve the exact efficiencies as indicated in the Table S2 for other sets. The reasons are TBC values for 2D-3D interfaces vary over a range of two orders of magnitude, and there has yet experimental and calculated works on different process parameters on same 2D material-substrate. However, these serve as a guideline and the underlying physics would help for an experimental effort for thermal efficiencies. Our analysis suggests that thermal efficiencies in 2D materials based devices (mostly dominated by TBC) could be improved by either increasing contact at the interface between two constituent materials, and/or by forming bonding at the interface. There is not yet a roadmap for processes that would improve the thermal efficiencies of the 2D material based devices despite experimental and theoretical advances in TBC between 2D-3D interface. Nor does a clear guideline for ideal material combination of 2D material and substrate yet from the thermal efficiencies point of view.

Concomitantly, *intrinsic factors* are related to the details of the vdW layer interactions, where additional layers to the monolayer moiety could increase the TBC, *e.g.*, the TBC of multilayer graphene/SiO<sub>2</sub> was recorded to be  $\sim$ 50 MW/m<sup>2</sup>. K – a factor of two increased from that for the SLG [19]. Additional layers act as a superstrate and enhance interfacial transmission through cross-plane flexural phonon branches. A similar trend was observed for MoS<sub>2</sub> and WSe<sub>2</sub> where TBC of monolayer MoS<sub>2</sub>/SiO<sub>2</sub> at  $\sim$ 11.5 MW/m<sup>2</sup>. K was smaller compared to the 13 MW/m<sup>2</sup>. K, at three layers [74]. As indicated earlier, the surface as well as interfacial bonding would also be relevant.

A low TBC at the interface of graphene/SiO<sub>2</sub>, considering the *intrinsic factors* alone, may be due to the low probability of phonon transmission from SiO<sub>2</sub> to graphene, due to the smaller number of phonon modes in SiO<sub>2</sub> (at<4THz) and the frequency mismatch, both of which result in reduced heat coupling across the interface Consequently, we analyzed the phonon dispersion diagrams and phonon density of states (PDOS) of (i) graphene, (ii) SiO<sub>2</sub>, and (iii) Si: Fig. 4. For these calculations, we assume a fourth-order polynomial fit to the experimental phonon dispersion of graphene [75], SiO<sub>2</sub> and Si [76]. While it was previously indicated, in literature, that the TBC of SLG/SiO<sub>2</sub> is lower than that of the Si/SiO<sub>2</sub> (~30%) in low frequency region - see inset of Fig. 4(d). Therefore, predicting the trend of TBC based on PDOS overlap may not be sufficient for various materials including SLG/SiO<sub>2</sub>.

In this context, we note that TBC is influenced by PDOS,  $v_{g}$ ,  $\omega_{max,j}$ ,



**Fig. 4.** Phonon dispersions and phonon density of states of (a) graphene, (b)  $SiO_2$  and (c) Si. Dispersion curves were fitted by polynomial equations (lines) from experimental data [47,48]. Solid lines and filled points represent *acoustic phonon* branches, while the dashed lines and unfilled points relate to the *optical phonon* branches. (d) Phonon related DOS of graphene,  $SiO_2$  and Si. The inset shows overlap of the DOS at low frequency.

and the mode transmission, *i.e.*,  $\alpha$ .While PDOS,  $v_g$ ,  $\omega_{max,j}$ , are inherent properties of material,  $\alpha$  depends on both materials across the interface. The PDOS of SLG is about an order of magnitude higher than that of Si at frequencies below ~4THz, and may broadly be attributed to the low  $v_g$  of ZA phonons, with concomitantly larger number of vibration modes compared to Si. Therefore, higher PDOS overlap between SLG and SiO<sub>2</sub> implies that there are more phonon modes of graphene available to interact with the phonon modes of the SiO<sub>2</sub>. However, the probability of phonon transmission across the interface (determined by  $\alpha$ ) depends on PDOS as well as  $v_g$  and  $\omega_{max, j}$ , which is higher for Si/SiO<sub>2</sub> interface. The average  $v_g$  of Si is a factor of two larger than that of graphene, *i.e.*, 6533m/s and 3200m/s respectively, and the  $\omega_{max, j}$  for Si are similar to SiO<sub>2</sub> compared to graphene, *i.e.*,  $\omega_{max}$  of SiO<sub>2</sub> is ~5THz. As a result the phonon transmission at SLG/SiO<sub>2</sub> interface.

Moreover, the ZA flexural mode of the graphene [77], see Fig. 4(a), has reduced phase velocity matching possible across the interface. Such correlation of TBC with the dispersion match reveals potential design trade-offs between efficient heat flow in graphene-based device. Although graphene is cited for superior thermal properties, it presents a high thermal resistance due to the phonon dispersion mismatch with other materials.

From an analysis of the component-wise contribution to the total TBC of the graphene-SiO<sub>2</sub>-Si stack in Fig. 3(b), it was found that the major contribution to the *R* arises from the two interfacial resistances, contributing to ~95% of the *net* value. The SLG/SiO<sub>2</sub> interface resistance is the largest contributor at ~62% of the *net R*, twice that of the SiO<sub>2</sub>/Si interface, and presents a potential bottleneck for heat flow in the stack. The obtained *R* is similar to what was found for other 2D material related stacks, *e.g.*, of ~6 x 10<sup>-8</sup> m<sup>2</sup>K/W in the MoS<sub>2</sub>/SiO<sub>2</sub>/Si stack [35].

Based on our analysis, we present a guideline on effect of materials and layouts on thermal efficiencies of 2D material based device. From our results, we find that thermal efficiencies of 2D material based device strongly depends on combination of 2D material's vibrational frequency of flexural mode as well as substrate's group velocity, Debye temperature, and thermal conductivity. We categorize the choice of material on two parts:

(a) Choice of substrate: For a particular 2D material, TBC will depend on substrate low frequency phonons to couple with 2D material's low frequency phonons. We can correlate this coupling in terms of physical parameters of the substrate like group velocity, Debye temperature and thermal conductivity. Substrates with high sound velocity, Debye temperature and thermal conductivity substrate generally results low TBC and hence has low thermal efficiencies of the device. For example, Diamond has the lowest TBC among the materials owing to its high sound velocity, Debye temperature and thermal conductivity (~9500m/s, 2250K and 2200W/m.K respectively). When diamond is replaced with AlN [78], the substrate the sound velocity, Debye temperature and thermal conductivity decrease (~4800m/s, 1150K and 321W/m. K [70] respectively), which results to a decrease in the TBC (see Fig. 2). Therefore, substrates that have low sound velocity, low Debye temperature, and low thermal conductivity are better for thermal efficiencies.

(b) choice of 2D material: If the substrate of an interface is fixed, the choice of 2D material will depend on its vibrational frequency of the flexural branch. 2D with lighter atomic mass and a small phonon bandwidth exhibits higher phonon DOS (PDOS) and results in higher TBC. For example, the higher TBC of h-BN/SiO<sub>2</sub> (Fig. 2(a)) over other 2D materials can be explained by its lighter atomic mass and its softer flexural phonon dispersion [5]. The two atom (B and N) basis in h-BN separates the acoustic energy bands from optical phonon bands and results a flattening of phonon dispersion [15,79]. This flatter dispersion leads to larger PDOS at low frequencies. Lighter atomic masses of h-BN also maximize the scattering rate with the substrate [33]. Therefore, it is hypothesized that compound 2D materials with atomic mass difference and a flatter flexural branch with smaller phonon bandwidth would exhibit higher thermal efficiencies.

The layout of 2D material would also affect thermal efficiency of a device. There are two types of interface layout in 2D materials based devices: side contact and edge contact [80]. Side contacts are made by contacting the plane of 2D materials with the surface of the substrate. This creates a large contact area at the interface which leads to a reduction in TBC. Typical values of TBC for side contacts are 10-100  $MW/m^2K$  (see Fig. 2(a)), which is an order of magnitude smaller compared to many common contacts in semiconductor devices, for example, the Au-Si (188 MW/m<sup>2</sup>K), Al-Si (450 MW/m<sup>2</sup>K), and Cu-Si (4108  $MW/m^2K$ ) interfaces [10]. Therefore, for 2D devices with side contact, the interfacial thermal resistance is an impediment to thermal efficiencies. On the other hand, for edge contact configuration, one-dimensional interface between 2D material and substrate leads to stronger overlapping of electronic orbitals between the 2D material and substrate, which can lead to a substantial increase in TBC [81]. Moreover, TBC also depends on surface orientation and contact direction [36]. For example, MoS<sub>2</sub>/Au edge contact was studied in three Au surfaces ((001), (110) and (111)) and contact line angles ( $0^\circ$ ,  $30^\circ$  and  $90^\circ$ ) using molecular dynamics simulations. The largest value of TBC (221

 $MW/m^2K$ ) was found to be at the (110) surface and at contact line angle 0° [36]. Therefore, the edge contact between a 2D material and 3D substrate has advantages in thermal efficiencies compared to the side contact layout.

Lastly, we comment on length dependence on interface thermal resistance and intrinsic thermal resistance of device components. The intrinsic thermal resistance of a component mainly depends on its thermal conductivity,  $\kappa$  and its lateral thickness, t. The interfacial thermal resistance between typical 2D material-substrate is of the order of  $10^{-8}\ \text{m}^2\text{K/W}.$  Therefore, if the arrangement of a 2D material or/and a substrate is such that the ratio of  $t/\kappa$  is greater than interface resistance, in that cases the intrinsic thermal resistance would no longer be negligible and even dominant. For 2D materials, the typical thickness is less than a nm, and typical  $\kappa$  varies from 1 to 1000 W/m<sup>2</sup>.K. One exception would be if the thickness if very large, for example organic layers or hybrid materials with very low  $\kappa$ , in that case intrinsic 2D would be dominant. For low  $\kappa$  substrates, lateral thickness greater than 100nm would make the substrate dominate resistance in the system. Lastly, If TBC of a 2D material and substrate is very high, ( $\sim 100W/m^2K$ ), the intrinsic thermal resistance of 2D material or the substrate could be limiting the thermal efficiencies of the device. For graphene/SiO<sub>2</sub>(1 nm)/Si (100 nm), the  $R^{SLG}$ ,  $R^{SiO_2}$ ,  $R^{Si}$ ,  $R^{SLG/SiO_2}$ ,  $R^{Si/SiO_2}$ ). are  $1 \times 10^{-9}$  m<sup>2</sup>. K/W,  $3.3 \times 10^{-9}$  m<sup>2</sup>. K/W,  $5.1 \times 10^{-8}$  m<sup>2</sup>. K/W and  $2.6 \times 10^{-8}$  m<sup>2</sup>. K/W respectively. Therefore, the geometry for intrinsic resistances to be comparable to interfacial thermal resistances would be if the thickness of graphene is  $\sim$ 60nm (graphite), or SiO<sub>2</sub> and Si thickness are on the order of 100nm. See Figure S1, S2 and S3 for thickness dependent intrinsic resistances.

#### 3. Conclusions

The present study provides a guide for energy-efficient design and thermal management of 2D material-based devices. Through a detailed consideration of the phonon frequency dispersion with respect to the thermal resistance and the related TBC, it was determined that the SLG/ SiO2 interface dominates heat flow in a SLG/SiO2/Si stack. Such an arrangement was investigated in the context of possible future 2D materials related electronics integration. The intrinsic thermal resistance as related to the ratio of the length scale and the  $\kappa_{2D}$  becomes less significant at the nanoscale. The high interfacial thermal resistance is attributed to weak bonding as well as incommensurate phonon frequency dispersion of the materials, on either side of the interface. It was also noted, through the presented work as well as from a survey of various 3D/3D and 2D/3D materials, that the interfaces in the former case have a larger TBC. It is indicated that the net R (/TBC) can be reduced (/increased) by choosing a substrate with phonon state frequencies matching/encompassed by the flexural phonon mode of the 2D material. Based on the analysis, guidelines on effect of materials and layouts on thermal efficiencies of 2D material-based device is indicated.

# Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

# Data availability

Data will be made available on request.

# Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.ijthermalsci.2022.107623.

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