

# Sub-0.5 nm Interfacial Dielectric Enables Superior Electrostatics: 65 mV/dec Top-Gated Carbon Nanotube FETs at 15 nm Gate Length

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**Abstract**—To realize superior electrostatic control, a gate oxide bilayer for carbon nanotubes (CNT) is employed consisting of a 0.35 nm interfacial dielectric ( $k=7.8$ ) and 2.5 nm high- $k$  ALD dielectric ( $k=24$ ). Using experimentally measured dielectric constants on  $sp^2$  carbon and minimum oxide thickness on CNT, a  $C_{OX}$  on CNT of  $2.94 \times 10^{-10}$  F/m is calculated for top-gate geometry. Gate leakage sub-1 pA/CNT is measured at 0.7V, better than the sub-5 nm node technology target. Top-gated carbon nanotube field effect transistors in this paper have 65 mV/dec subthreshold slope and DIBL as low as 20 mV/V at 15 nm gate length. Negligible hysteresis and no degradation in drive current from the top-gate process is observed. TCAD modeling predicts this approach will enable 68 mV/dec for top-gate CNFET with 10 nm  $L_G$ , 1 nm CNT diameter and 250 CNT/ $\mu m$ , revealing a path to energy and performance gains from a CNT transistor technology.

## I. INTRODUCTION

Carbon nanotube field-effect transistors (CNFETs) are a candidate logic transistor to extend density, efficiency, and performance improvements beyond the limits of conventional Si CMOS. This is enabled by the  $\sim 1$  nm thin CNT body, high mobility/velocity, and lower parasitic capacitance [1]. CNFETs can be processed entirely at sub-400 °C enabling monolithic 3D integration of logic and memory with dense interconnectivity [2]. However, it has been challenging to fabricate the top-gate or surround-gate CNFETs for high performance applications due to fundamental obstacles in nucleating conventional high- $k$  atomic layer deposited (ALD) gate dielectrics on defect-free  $sp^2$  bonded carbon surfaces. Fig. 1a-c highlights typical defect and step edge nucleation for ALD films on Highly Oriented Pyrolytic Graphite (HOPG), which has the same  $sp^2$  carbon surface as CNT. To work around this obstacle, previous short-channel CNFETs relied on approaches summarized in Table I [3-8]. The thick gate oxide ( $t_{OX}$ ), low oxide capacitance ( $C_{OX}$ ), and stability obstacles of these previous approaches limits CNFET performance, scalability, and robustness.

## II. THIN HIGH-K DIELECTRICS ON CARBON NANOTUBE

This work overcomes these limitations with a very thin interfacial layer dielectric (ILX) composed of  $Al_2O_3$  deposited by the low temperature “nanofog” method [10] that is compatible with  $sp^2$ -carbon surfaces such as CNT. Fig 1d

shows 10 cycles of ILX (1.25 nm measured by TEM) conformably coating HOPG as a nucleation template for high- $k$  ALD. Fig 1e shows a dielectric bilayer on a CNT consisting of 6 cycles of ILX ( $\sim 0.65$  nm) and 20 cycles of  $HfO_2$  ( $\sim 2.5$  nm) forms a continuous film on top of the CNT, demonstrating ILX nucleates readily on the CNT and enables conventional high- $k$  ALD materials to be used for the CNT gate stack.

To understand the properties of this dielectric bilayer, the dielectric constants and minimum thickness of each layer must be measured. The dielectric constants of experimental ILX and  $HfO_2$  layers with a TiN/Ti/Pd gettering gate were extracted from  $C_{OX}$  versus thickness series on HOPG (Fig 2). TEM cross-section inspection of bilayer in Fig 2b inset is used to verify the dielectric film thicknesses on HOPG. Experimental values of  $k_{HfO_2} = 24.0$  from the capacitance versus  $t_{HfO_2}$  slope, and  $k_{ILX} = 7.8$  from the  $t_{HfO_2} = 0$  intercept were determined.

The minimum thickness of ILX and  $HfO_2$  on CNT is bounded by gate leakage current. To ensure that gate leakage current does not dominate circuit stand-by power, gate leakage per CNT at  $V_{GS} = V_{DD}$  ( $I_{G,ON}$ ) should be less than 10% of drain leakage per CNT at  $V_{GS} = 0V$  ( $I_{D,OFF}$ ) [11]. The target  $I_{G,ON} = 1$  pA/CNT for a 10 nm  $L_G$ , was determined from TCAD-based power-performance analysis that identifies multiple design options with significantly improved speed and efficiency over TSMC’s sub-5 nm node Si CMOS [12]. A gate leakage test structure was fabricated on aligned CNTs on quartz as described in Fig. 3. To ensure that ILX nucleates on  $sp^2$  carbon and not on process residues, ILX is deposited on pristine CNTs that have seen no processing after CNT chemical vapor deposition growth. Table II summarizes the bilayer conditions studied, CNT density, device dimensions, and the percentage of devices that meet the leakage target. Fig. 4 shows the measured  $I_G$  data for a representative chip with up to 104 devices per chip each normalized to a single CNT with 10 nm  $L_G$ . For devices with 2 cycles of ILX and 20 cycles of  $HfO_2$ , incomplete dielectric coverage results in less than 3% of the devices meet the leakage specification— indicating bilayer with highest achievable  $C_{OX}$  using this method. TEM in Fig. 5 measures an ILX thickness of 0.35 nm and a  $HfO_2$  thickness of 2.5 nm from 4 cycles of ILX and 20 cycles of  $HfO_2$ . These devices used a non-gettering gate, but a repeat leakage test with TiN/Ti/Pd gate metal as used in  $k$ -value extraction resulted in similar leakage.

### III. SHORT CHANNEL TOP-GATE CNFETs

To validate the usefulness of ILX on CNT, top-gate CNFETs were fabricated with  $L_G$  from 100 nm to 15 nm. The top-gate (TG) CNFET device structure is illustrated in Fig. 6. The BG is used to apply a negative bias to the extension region of the CNFET during TG measurements, using electrostatic doping to create a P-N-P carrier profile along the CNT in the off-state. In Fig 6b-c the 15 nm  $L_G$  is verified by SEM and TEM cross-section on a device displaying 65 mV/dec sub- $V_T$  slope. The top-gate CNFET devices were fabricated with a dielectric bilayer consisting of 10 cycles ILX (~1.25 nm) and 20 cycles of  $\text{HfO}_2$  (~2.5 nm), and a non-gettering gate, which is relaxed from the  $t_{\text{ILX}}$  limit identified by gate leakage in previous section. TG leakage is below measurement noise floor across the +/- 1.5V sweep range. Fig. 7a shows the  $I_D$ - $V_{GS}$  characteristics for the same CNFETs at different stages of fabrication. Critically, the CNT current is not degraded by dielectric deposition as often occurs with conventional ALD on CNTs [6]. Ambipolar current is suppressed for TG CNFETs as the BG firmly sets the CNT potential near the metal-semiconductor Schottky-contact. Fig 7b shows an example CNFET  $I_D$ - $V_{GS}$  ( $L_G = 100$  nm) with 60 mV/dec sub- $V_T$  slope and <20 mV/V DIBL. A  $V_{GS}$  sweep range of 0.7V is indicated, suggesting ILX enables  $V_{GS}$  and  $V_{DS}$  operation with nominal  $V_{DD}$ . Fig 7c plots  $I_D$ - $V_{DS}$  behavior with saturation across a 200 nm contact separation at >10  $\mu\text{A}$  per CNT at -0.75V  $V_{DS}$ .

Short-channel effects are considered in Fig. 8 by measuring sub- $V_T$  slope versus gate length. TG devices display 60-70 mV/dec for all physical  $L_G$  from 100 nm to 15 nm, confirming excellent gate control and suggests low  $D_{IT}$ . Two example devices with 15 nm  $L_G$  display DIBL below 20 mV/V in Fig. 8b and sub- $V_T$  slope of 65 mV/dec in Fig 8c. In Fig. 9 an unpassivated CNFET initially has hysteresis  $\Delta V_T \approx 2\text{V}$  across +/- 3V  $V_{BG}$  sweep range. After TG fabrication, due to improved  $C_{OX}$  the  $\Delta V_T$  from hysteresis is reduced to below the noise level (due to oxide traps) across a 0.5V  $V_{GS}$  sweep range for high performance logic. Electrostatics will be significantly improved in future CNFETs by thinning ILX from 1.25 nm to 0.35 nm as demonstrated in leakage test structures (Section II).

### IV. ELECTROSTATICS MODELING DOWN TO 10 NM $L_G$

Thin-body cylindrical channel materials such as CNT fundamentally cannot use simple capacitance figures of merit (such as equivalent oxide thickness, EOT) because:

- 1) Complex transistor geometries (BG, TG, DG, and SG from Fig 10) and multiple device parameters (e.g.  $d_{\text{CNT}}$ , total  $t_{\text{OX}}$ ,  $P$ ,  $L_G$ ,  $L_{\text{EXT}}$ ,  $N_{\text{EXT}}$ , etc...) **strongly** influence the gate electrostatic control over the CNT channel. A simple approximation has yet to be defined.
- 2) In a cylindrical channel,  $C_{OX}$  is primarily limited by interfacial layer properties  $t_{\text{ILX}}$  and  $k_{\text{ILX}}$  due to electric field profile  $\propto 1/(k_{\text{OX}}R)$  (Fig 11a). Therefore planar EOT  $\propto k_{\text{OX}}/t_{\text{OX}}$  intuition does not apply. For example, interchanging the order of the  $k$ -value of the bilayer for planar gate geometry gives the same  $C_{OX}$ , but the cylindrical geometry gives different values of  $C_{OX}$ .

- 3) The  $t_{\text{OX}}$  is thicker than the channel body of ~1 nm  $d_{\text{CNT}}$  so fringing fields through gate oxide dominate short channel effects. Therefore, total gate physical  $t_{\text{OX}}$  is a key figure of merit in addition to  $C_{OX}$ .

For example, Fig 11b-c compares the thicker  $\text{ZrO}_2$  dielectric film ( $t_{\text{OX}} = 8$  nm,  $k = 25$ ) from ref. 8 to this work in a TG TCAD model. The calculated  $C_{OX}$  for both structures is nearly identical, with  $2.8 \times 10^{-10}$  F/m for ref. 8 and  $2.9 \times 10^{-10}$  F/m in this work with CNT pitch ( $P$ ) of 15 nm. Fig. 11b shows the potential drop due to fringing field from the drain contact is worsened by thick dielectric. Similarly, Fig 11c compares screening effects from dense CNT ( $P = 4$  nm) to sparse CNT ( $P = 15$  nm). Thick oxide has degraded electrostatic control in the regions between the dense CNT compared to thin oxide.

TCAD modeling is used to evaluate whether a gate dielectric sufficiently asserts gate control over the semiconducting channel in the off-state. To focus on electrostatic control as a function of gate oxide, this modeling work has decoupled tunneling leakage. Modeling results are summarized in Fig 12 and Table I for this work and Ref. 3,4,6 and 8. Fig 12a models sub- $V_T$  slope versus gate length illustrating TG, DG, and SG geometries offer superior electrostatic control compared to BG as the gate length approaches 10 nm, demonstrating the need for a gate dielectric deposition process on CNT. In Fig. 12b the sensitivity of CNFET sub- $V_T$  swing at  $L_G = 10$  nm is modeled considering gate geometry (BG, TG, DG, SG), CNT density ( $P = 15$ ,  $P = 4$ ), and high- $k$  film thickness (2-5 nm dielectric  $k = 25$ , on 1 nm ILX with  $k = 8$ ). For ILX = 1 nm, only DG and SG structures appear feasible to deliver sub-70 mV/dec for 250 CNT/um. The 8 nm  $\text{ZrO}_2$  film ( $k = 25$ ) from ref. 8 with similar  $C_{OX}$  only delivers 97.8 mV/dec, highlighting the importance of simultaneously large  $C_{OX}$  and small  $t_{\text{OX}}$ . With the ILX and  $\text{HfO}_2$  oxide bilayer demonstrated in this work for a TEM-measured thickness and electrically measured dielectric constant (with gettering gate),  $t_{\text{ILX}}$  0.35 nm ( $k = 8$ ) and  $t_{\text{HfO}_2}$  of 2.5 nm ( $k = 24$ ), the calculated sub- $V_T$  slope for  $P = 4$  nm is 68 mV/dec. This approach can be further improved with a SG geometry.

### ACKNOWLEDGMENT

The authors thank C. Diaz and A. Kumar. Work supported by Stanford SNF and SNSF NSF award ECCS-1542152; UCSD Nano3 NSF award EECS-1542148; Stanford SystemX and DARPA 3DSoc. TEMs by S. L. Liew, and Y.C. Liang.

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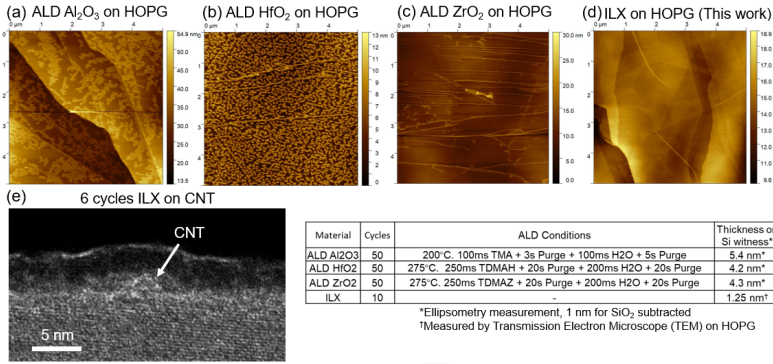


Fig. 1. Conventional ALD does not nucleate on  $sp^2$  carbon surfaces, ILX forms a nucleation layer for  $HfO_2$  ALD. (a-c) AFM images showing ALD  $Al_2O_3$ ,  $HfO_2$ , and  $ZrO_2$  nucleate on defects or step edges, remains discontinuous even after 50 cycles on HOPG. (d) ILX after only 10 cycles (1.25 nm) is conformal and pinhole free on HOPG. (e) 6 cycles of ILX (~0.65 nm) forms continuous film on pristine aligned CNT as nucleation layer. 20 cycles of  $HfO_2$  (~2.5 nm) forms continuous film on CNT. Standard process conditions are used for each ALD sample on HOPG.

Reference	Geometry (Fig. 10)	Interfacial Material Thickness & Dielectric constant	High-k Material Thickness & Dielectric constant	$C_{ox}$ from TCAD (P=15 nm)	$C_{ox}$ from TCAD (P=4 nm)	Advantages	Limitations
Ref. 3 IBM 2012	Back-Gate (SG)	-	$HfO_2$ 3 nm $k = 18$	$1.54 \times 10^{10}$ F/m (BG)	$1.04 \times 10^{10}$ F/m (BG)	• Avoids ALD challenge on CNT	• Lower electrostatic control vs. TG, DG, SG. (Fig 12)
Ref. 4 PKU 2017	Top-Gate (TG)	Electron Beam Induced (EBID) Carbon < 1 nm $k \sim 3.3$ [13]	$HfO_2$ 3.5 nm $k = 18$	$1.3 \times 10^{10}$ F/m (TG)	$7.3 \times 10^{11}$ F/m (TG)	• Realize thin ALD oxide on CNT	• Low-k carbon severely degrades $C_{ox}$ (Fig 11) • Carbon residue is not manufacturable
Ref. 6 IBM 2013	Surround-Gate (SG)	$Al_2O_3$ 1.5 nm $k_{eff} \sim 8.5$	$HfO_2$ 8 nm $k_{eff} \sim 8.5$	$1.63 \times 10^{10}$ F/m (SG)	$1.63 \times 10^{10}$ F/m (SG)	• Overcomes nucleation problem SG geometry has best electrostatics.	• Low $k_{eff}$ reported for total film, limits $C_{ox}$ • Requires 50 cycles for continuous interfacial dielectric. • Oxide bilayer is too thick, degrades electrostatic control for dense CNTs
Ref. 8 Stanford 2002	Top-Gate (TG)	-	$ZrO_2$ 8 nm $k=25$	$2.8 \times 10^{10}$ F/m (TG)	$9.8 \times 10^{11}$ F/m (TG)	• Avoids ALD challenge on CNT by overgrowing from substrate and defects. • High $C_{ox}$ without interfacial layer	• Does not work for SG. Nucleation at defects degrades mobility. • Requires thick oxide, which degrades electrostatic control.
This work	Top-Gate (TG)	$Al_2O_3$ Nanofog 0.2-0.5 nm $k = 7.8$	$HfO_2$ 2.5 nm $k = 24$	$2.94 \times 10^{10}$ F/m (TG)	$1.87 \times 10^{10}$ F/m (TG)	• High $C_{ox}$ and oxide bilayer is thin. • Interfacial layer is relatively high-k • Compatible with SG • Continuous in 4 cycles or less	-

Table I: Summary of existing approaches and this approach to nucleate thin high-k dielectric on CNT, including materials parameters,  $C_{ox}$  simulated from TCAD models (same assumptions in Fig 12, and simulation uses same gate geometry used in the reference), and an analysis of advantages and limitations.

Chip #	ILX # Cyc	HfO2 # Cyc	# CNT per device	$L_G / W$ ( $\mu m$ )	% Devices $I_G < 1$ pA/CNT at $V_{GS} = 0.7$ V
1	10	40	180	5 / 100	>85%
2	10	30	106	5 / 100	75%
3	10	20	91	5 / 100	60%
4	8	20	175	5 / 100	57.5%
5	6	20	134	5 / 100	85%
6	4	20	24	5 / 100	50%
7	2	20	86	5 / 100	< 3%

Table II. Summary of experimental dielectric bilayer conditions in leakage measurements on pristine CNTs. Steep decrease in % of devices that meet a 1 pA/CNT gate leakage specification at 0.7V  $V_{DD}$  between 4 cycles of ILX and 2 cycles of ILX, indicating 4 cycles is the thickness limit of ILX for this bilayer due to incomplete coverage of the CNT.

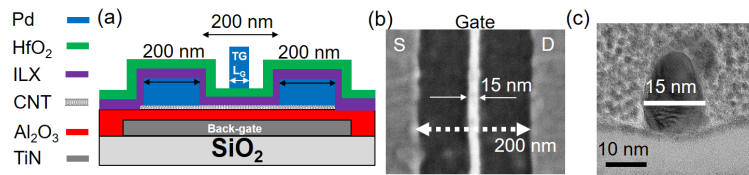


Fig. 6. (a) Device structure for short-channel top-gate CNFETs with electrostatically doped extensions through back-gate. (b) SEM image of top-gate CNFET with 15 nm  $L_G$  and labeled source, drain and gate electrodes. (c) Cross-section TEM validating  $L_G$  of 15 nm on CNFET with Sub- $V_T$  slope of 65 mV/dec.

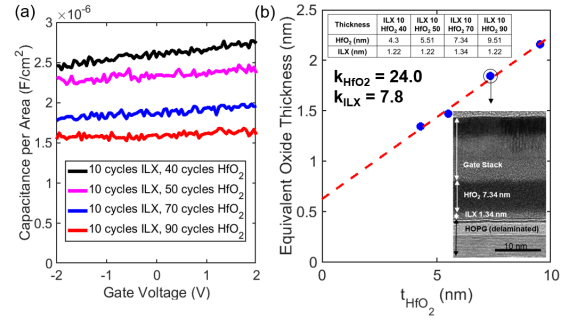


Fig. 2. Experimental determination of  $k$ -values for bilayer oxide. (a) Capacitance per unit area at 50 kHz for various thickness of  $HfO_2$  on 1.25 nm ILX on  $sp^2$  carbon surface of HOPG substrate. Leakage current density is negligible for all samples. (b) Equivalent oxide thickness (EOT) versus  $HfO_2$  thickness. Extracted  $k$ -values of  $HfO_2$  is 24.0, and ILX is 7.8.

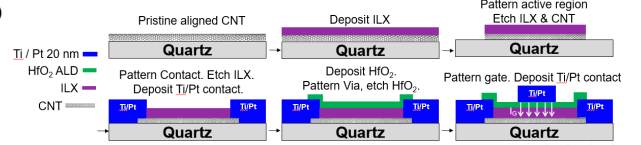


Fig. 3. Process flow for gate leakage measurement test structure on pristine CNTs. Top row: (1) Pristine aligned CNT grown on quartz. (2) Deposit ILX (thickness in Table II). (3) Remove ILX and CNTs from outside active region. Bottom row: (4) Pattern contact electrodes, etch ILX within contact region, evaporate then liftoff 1 nm Ti and 20 nm Pt. (5) ALD  $HfO_2$  (thickness in Table II). Pattern via and etch  $HfO_2$ . (6) Pattern gate electrode, evaporate then liftoff 1 nm Ti and 20 nm Pt. The gate length is 5  $\mu m$  and the extension length is 2.5  $\mu m$  per side for data reported in this paper.

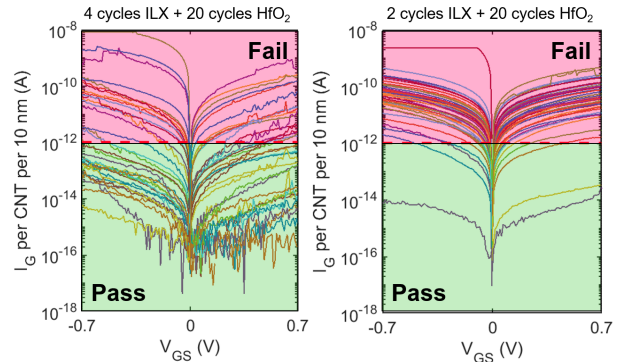


Fig. 4. A sharp decrease in yield marking thickness limit is observed from  $I_G$  vs  $V_{GS}$  data for, normalized for a single CNT across 10 nm  $L_G$  Chip 6 with 4 / 20 cycles of ILX /  $HfO_2$  and Chip 7 with 2 / 20 cycles of ILX /  $HfO_2$ . Horizontal line indicates single-CNT leakage target for 10 nm  $L_G$  CNFET. Note: Ti/Pt gate here differs from TiN/Pd gate used for  $k$ -value extraction. Repeated test using TiN/Ti/Pd gate resulted in similar leakage.

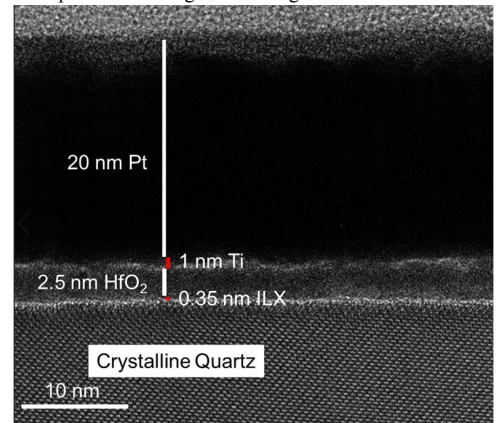


Fig. 5. HRTEM of Chip 6 (Table II) with 4 cycles ILX and 20 cycles  $HfO_2$ . Layer thicknesses are 0.35 nm for ILX and 2.5 nm for  $HfO_2$ .



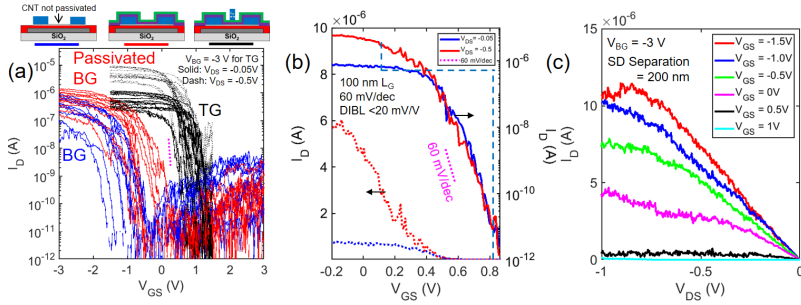


Fig. 7. Top-gate CNFET IV data (a)  $I_D$ - $V_{GS}$  for 13 CNFETs progressing through fabrication: blue uses TiN back-gate (BG) and CNTs are unpassivated, red is TiN BG with 10 cycles ILX and 20 cycles  $HfO_2$  without top-gate, and black the CNTs are measured by biasing the Pd top-gate (TG).  $I_{ON}$  and  $I_{OFF}$  are not degraded, Sub- $V_T$  slope is improved (60 mV/dec indicated in magenta), and  $V_T$  shifts +2V. (b) Example 100 nm  $L_G$  CNFET with 60 mV/dec sub- $V_T$  slope and < 20 mV/V DIBL. A  $V_{DD} = 0.7V$  gate sweep range (cyan dashed lines) indicated for symmetric  $V_{DS} = V_{GS}$  operation starting from 10 pA/CNT off-current. (c) Example  $I_D$ - $V_{DS}$  -0.75V across 200 nm separation between SD with maximum current >10  $\mu A$  for a single CNT.

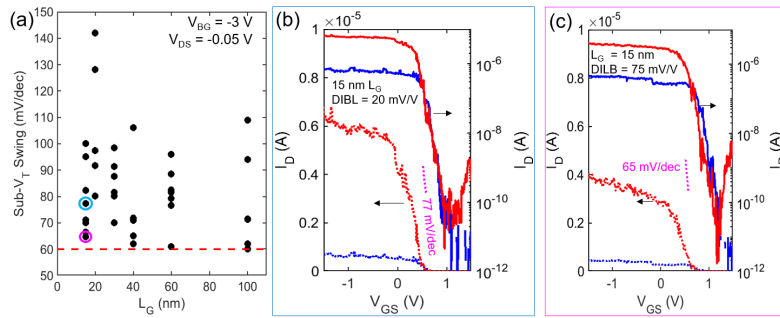


Fig. 8. Electrostatic control in top-gate CNFETs. (a) Sub- $V_T$  Slope versus gate length, with 65 mV/dec achieved down to 15 nm  $L_G$  and several instances of 60 mV/dec at longer gate lengths. Sub- $V_T$  slope averaged across >180 mV of  $V_{GS}$  range. (b)  $I_D$ - $V_{GS}$  of 15nm  $L_G$  CNFETs with 20 mV/V of DIBL. (c)  $I_D$ - $V_{GS}$  of a 15 nm  $L_G$  CNFET with 65 mV/dec of sub- $V_T$  slope. Future improvements in electrostatic control are likely when shrinking ILX gate dielectric from 1.25 nm to 0.35 nm. Note:  $L_{CH}$  in off-state is larger than physical  $L_G$  with low extension doping. Note 2: Precision in extracting sub- $V_T$  swing and DIBL is often limited by trap noise which may shift  $V_T$  during measurement, as seen in (c).

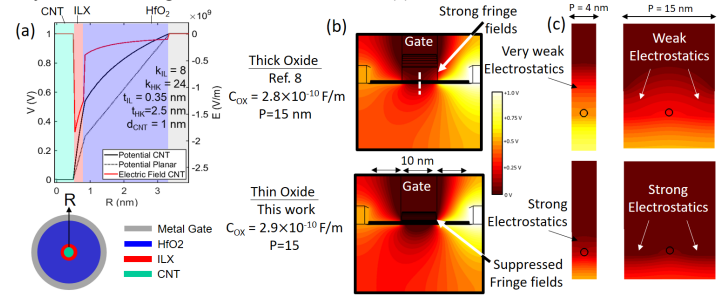


Fig. 11. Gate dielectrics to cylindrical channel are best evaluated by two metrics:  $C_{OX}$  and total oxide thickness. (a) Radial profile of potential and electric field in cylindrical bilayer dielectric from COMSOL simulation illustrating interfacial layer limiting  $C_{OX}$  with  $k_{ILX}$  and  $t_{ILX}$  account for 53% voltage drop with only 12% of thickness. A planar capacitor would have only 30% voltage drop in ILX region. (b) In CNT  $t_{OX} \gg d_{CNT}$  so fringe fields from drain and source extensions degrade sub- $V_T$  slope travel mostly through gate dielectrics. Effect is worse for thick oxides even if total  $C_{OX}$  is similar (e.g. this work compared to Ref. 8). (c) Gate control between adjacent CNTs is significantly worse for thick dielectrics, particularly for dense CNT with  $P=4$ , due to screening effects between CNTs the gate must overcome to turn off the channel.

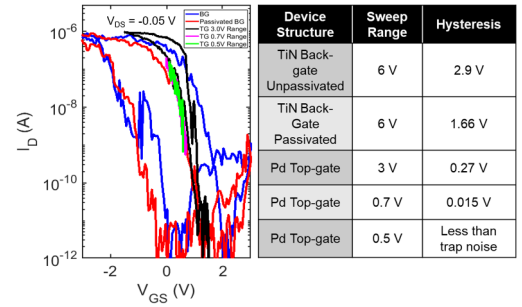


Fig. 9. Hysteresis in CNFET with BG (blue), BG with ILX and  $HfO_2$  passivation (red), and top gate with 3V (black), 0.7V (magenta) and 0.5V (green) of  $V_{GS}$  sweep range. The higher  $C_{OX}$  of TG significantly improves hysteresis. At 0.5V sweep range on TG, the  $\Delta V_T$  from hysteresis is less than noise observed due to trap effects.

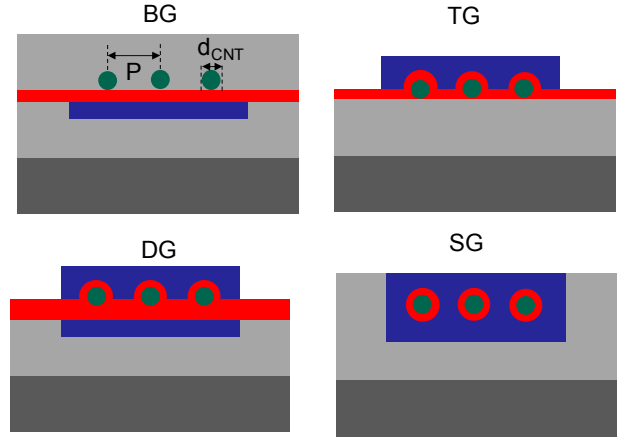


Fig. 10. Schematic CNFET geometries. TG, Double Gate (DG), and SG require a process capable to deposit thin, high-k, leakage free dielectric on top of  $sp^2$  carbon surface. Light grey is  $SiO_2$ , dark grey is Si substrate, blue is gate metal, red is ILX + high-k dielectric stack, green is CNT. CNT pitch ( $P$ ) and CNT diameter ( $d_{CNT}$ ) are key design parameters for CNFET drive current and energy efficiency optimization.

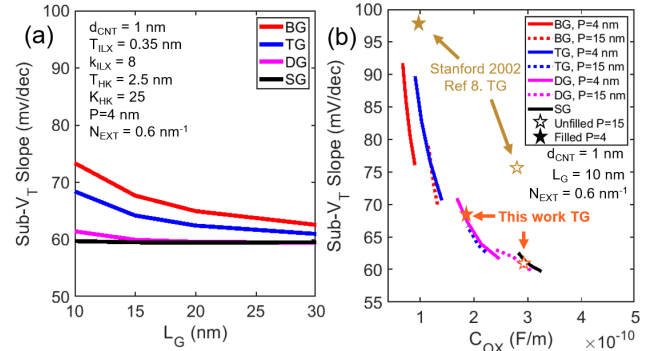


Fig. 12. 3D TCAD modeling results. (a) Short channel subthreshold slope behavior indicates that the top-gate, double-gate, and surrounding gate geometry have superior electrostatic control at short channel versus back-gate geometry, therefore a process to deposit dielectric on CNT is essential. (b) CNFET gate geometry, CNT density, and dielectric  $k$  and total thickness are critical parameters in determining sub- $V_T$  slope. For each curve we simulate  $T_{ILX} = 1$  nm,  $k_{ILX} = 8$  for  $k_{HK} = 25$  and  $T_{HK}$  from 2.5 nm with  $P=4$  and  $P=15$ .  $N_{EXT}$  is doping strength in the extension region. Note 1: SD tunneling and band-to-band tunneling are decoupled from this modeling, but the 1nm  $d_{CNT}$  and  $0.6$  nm $^{-1}$   $N_{EXT}$  are chosen in a regime in which these tunneling effects are suppressed. Note 2: Stars use dielectric thickness and  $k$  values from this work and ref 8.